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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/067,372	Applicant(s) WANG ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-75* is/are pending in the application.

4a) Of the above claim(s) *36-42 and 69-75* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35 and 43-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,6*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *7*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-35 and 43-68, drawn to A Method for Providing Ordered Capture Clocks to Detect or Locate Faults within N Clock Domains Comprising: Generating and Loading N Pseudorandom Stimuli to Scan Cells within the N Clock Domains; Applying an Ordered Sequence of Capture Clocks; and Compacting N Output Responses of all Said Scan Cells to Signatures; classified in class 714, subclass 732.

   II. Claims 36-42 and 69-75, drawn to A Computer-Aided Design (CAD) System Comprising the Computer-Implemented Steps of: Compiling HDL Code or a Netlist that Represents said Integrated Circuit or Circuit Assembly; Performing a Self-Test Rule Check; Performing a Self-Test Rule Repair; Performing Multiple-Capture Self-Test Synthesis; and Generating HDL Test Benches and ATE Test Programs; classified in class 714, subclass 741.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I; A Method for Providing Ordered Capture Clocks to Detect or Locate Faults within N Clock Domains Comprising: Generating and Loading N Pseudorandom Stimuli to Scan Cells within the N Clock Domains; Applying an Ordered Sequence of

Capture Clocks; and Compacting N Output Responses of all Said Scan Cells to Signatures; and Group II; A Computer-Aided Design (CAD) System Comprising the Computer-Implemented Steps of: Compiling HDL Code or a Netlist that Represents said Integrated Circuit or Circuit Assembly; Performing a Self-Test Rule Check; Performing a Self-Test Rule Repair; Performing Multiple-Capture Self-Test Synthesis; and Generating HDL Test Benches and ATE Test Programs; are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions Group I is a method for testing an integrated circuit using scan circuitry embedded in the integrated circuit and Group II is a method for simulating an integrated circuit.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Jim Zegeer on 21 June 2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-35 and 43-68. Affirmation of this election must be made by applicant in replying to this Office action. Claims 36-42 and 69-75 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '208', '209', '210', '233', '234', '250' & '251' in Figure 2; '601', '602', '604' &

'605' in Figure 6; and '701', '709', '710', '712', '713', '715', '716', '718' & '719' in Figure 7.

Note: the previous list of reference characters is provides an example of some of the drawing errors, but is not a comprehensive list by any means. The drawings are replete with errors. The Applicant must thoroughly review the drawings and correct all drawing errors.

Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-31, 43-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 30, 43 and 63 recite, "(d) repeating the steps of (a)-(c) until a predetermined limiting criteria is reached, wherein (a) and (c) occur substantially concurrently". It is not clear what "wherein (a) and (c) occur substantially concurrently" refers to, i.e. whether steps of (a)-(c) are repeated until (a) and (c) occur substantially concurrently or whether the statement "wherein (a) and (c) occur substantially concurrently" is independent of step (d).

Claims 12 and 50 recite, "another ordered sequence of capture clocks selectively longer or shorter than said ordered sequence of capture clocks" is incomprehensible. It is not clear whether "said ordered sequence" refers to "another ordered sequence" or a previously defined ordered sequence. It is not clear whether "longer or shorter" refers to the clocks, i.e., length of clock period, or whether it refers to the length of the sequence. The term "longer or shorter" is a relative term with and the Applicant has not provided a means or language to ascertain the relative degree.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4, 6, 10-20, 27, 30-35, 43-46, 48-60 and 63-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) in view of Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2).

35 U.S.C. 103(a) rejection of claims 1, 30-32, 43, 59 and 63-65.

Nadeau-Dostie1 teaches a method for providing capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N>1 and each domain has a plurality of scan cells (see Abstract in Nadeau-Dostie1), said method comprising the steps of: a. generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation (col. 24, lines 7-10 in Nadeau-Dostie1 teaches generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation); b. applying a sequence of capture clocks to all said scan cells within said N clock domains during the capture operation (col.8, lines 16-21 in Nadeau-Dostie1 teaches that the domain clocks are use to perform the capture operation: Note; ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a capture clock); c. compacting N output responses of all said scan cells to

signatures during the compact operation (see col. 7, lines 46-52 in Nadeau-Dostie1; Note: and MISR is a device for compacting N output responses of all said scan cells to signatures during the compact operation); and d. repeating the steps of a-c until a predetermined limiting criteria is reached, wherein steps a and c occur substantially concurrently (col.8, lines 16-21 in Nadeau-Dostie1 teaches that the domain clocks are use to perform the capture operation and launch the last bit of the test stimuli, hence steps a and c occur substantially concurrently; Note: col. 8, lines 12-16 in Nadeau-Dostie1 teaches that, prior to performing the capture operation and launch the last bit of the test stimuli, shifting in the test stimulus is performed concurrently with the capture operation: Note also signature analysis is a means for preparing output responses for signature analysis).

However Nadeau-Dostie1 does not explicitly teach the specific use of an ordered capture clocks.

Nadeau-Dostie2, in an analogous art, teaches an ordered sequence of clock signals (ck1, ck2 and ck3 in Figure 4 of Nadeau-Dostie2). The Examiner would like to point out that clocks from different clock domains require a means for identifying the clocks and associating them with their respective clock domains. Creating an ordered sequence of labels to identify the clocks and respective clock domains is a common way of identifying clock signals.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 with the teachings of Nadeau-Dostie2 by including use of an ordered capture clocks. This modification would have been obvious

to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an ordered capture clocks would have provided the opportunity for identifying the clocks and associating them with their respective clock domains.

35 U.S.C. 103(a) rejection of claims 2 and 44.

Nadeau-Dostie1 and Nadeau-Dostie2 teach that each said capture clock is programmable to contain one or more clock pulses for performing said shift/compact and capture operations on all said scan cells within one said clock domain (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within one said clock domain); wherein said clock domain is solely controlled by said capture clock (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 uses capture clock ClockHS to control all clock domain operations during testing); and said capture clock can be either generated internally or controlled externally (the capture clock ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can either generated internally or controlled externally depending on whether BistCLK and ClockHS-raw are internal or external signals), and can operate either at its rated clock speed (at-speed) or at a selected clock speed (ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can operate either at its rated clock speed ClockHS-raw or at a selected clock speed BistCLK).

35 U.S.C. 103(a) rejection of claims 3, 33, 45 and 66.

Nadeau-Dostie1 and Nadeau-Dostie2 teach providing N scan enable signals each within one said clock domain (SEHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1); wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds (see Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1).

35 U.S.C. 103(a) rejection of claims 4, 34, 46 and 67.

Nadeau-Dostie1 and Nadeau-Dostie2 teach said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock speed (SE[2] in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a global scan enable signal).

35 U.S.C. 103(a) rejection of claims 6, 27 and 60.

Nadeau-Dostie1 and Nadeau-Dostie2 teach the step of comparing said signatures with their expected signatures for error indication, after said predetermined limiting criteria is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit

assembly or shifting out said signatures for comparison in an ATE (col. 9, lines 25-28 in Nadeau-Dostie2).

35 U.S.C. 103(a) rejection of claims 10 and 48.

Nadeau-Dostie1 and Nadeau-Dostie2 teach performing said capture operation concurrently on a plurality of clock domains which do not have any logic block crossing each other (col 17, lines 23-35 in Nadeau-Dostie1).

35 U.S.C. 103(a) rejection of claims 11, 13, 14, 49, 51 and 52.

Nadeau-Dostie1 and Nadeau-Dostie2 teach the use of capture disable signals CD[0] and CD[1] in Figures 5 and 6, which allow for applying said capture clocks in a selected order for detecting or locating additional faults in said integrated circuit or circuit assembly.

35 U.S.C. 103(a) rejection of claims 12 and 50.

Nadeau-Dostie1 and Nadeau-Dostie2 teach various clocks operating at different speeds, i.e., longer or shorter periods.

35 U.S.C. 103(a) rejection of claims 15-20 and 53-58.

Nadeau-Dostie1 and Nadeau-Dostie2 teach selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-

Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within one said clock domain).

35 U.S.C. 103(a) rejection of claims 35 and 68.

Capture clock ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is the only clock use through out the test.

5. Claims 5 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) and Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2) in view of Nadeau-Dostie; Benoit et al. (US 6327684 B1, hereafter referred to as Nadeau-Dostie3).

35 U.S.C. 103(a) rejection of claims 5 and 47.

Nadeau-Dostie1 and Nadeau-Dostie2 substantially teaches the claimed invention described in claims 1-4 (as rejected above). In addition, Nadeau-Dostie1 and Nadeau-Dostie2 teach that each said capture clock is programmable to contain one or more clock pulses for performing said shift/compact and capture operations on all said scan cells within one said clock domain (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within

one said clock domain); wherein said clock domain is solely controlled by said capture clock (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 uses capture clock ClockHS to control all clock domain operations during testing); and said capture clock can be either generated internally or controlled externally (the capture clock ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can either generated internally or controlled externally depending on whether BistCLK and ClockHS-raw are internal or external signals), and can operate either at its rated clock speed (at-speed) or at a selected clock speed (ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can operate either at its rated clock speed ClockHS-raw or at a selected clock speed BistCLK).

However Nadeau-Dostie1 and Nadeau-Dostie2 do not explicitly teach the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption.

Nadeau-Dostie3, in an analogous art, teaches the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption (col. 8, lines 12-19, Nadeau-Dostie3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 and Nadeau-Dostie2 with the teachings of Nadeau-Dostie3 by including the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill

in the art would have recognized that the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption would have provided the opportunity to reduce power consumption.

6. Claims 7-9, 21-26, 28, 29, 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) and Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2) in view of Rajski; Janusz et al. (US 5991909 A, hereafter referred to as Rajski).

35 U.S.C. 103(a) rejection of claims 7 and 21.

Nadeau-Dostie1 and Nadeau-Dostie2 substantially teaches the claimed invention described in claims 1-6 (as rejected above).

However Nadeau-Dostie1 and Nadeau-Dostie2 do not explicitly teach the specific use of a plurality of PRPGs.

Rajski, in an analogous art, teaches use of a plurality of PRPGs (see Figure 6 in Rajski). Note also that each of the LFSR PRPG circuits in Figures 1 and 6 are connected to Combinational Phase Shifter logic between the LFSRs and the scan chains.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 and Nadeau-Dostie2 with the teachings of Rajski by including use of a plurality of PRPGs. This modification would have been

obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a plurality of PRPGs would have provided the opportunity to provide different and independent sets of pseudorandom test stimuli to different functional logic units.

35 U.S.C. 103(a) rejection of claim 8.

Nadeau-Dostie1, Nadeau-Dostie2 and Rajski teach a finite-state machine to automatically generate a number of test patterns; wherein said test patterns are applied through a phase shifter to a plurality of clock domains (see Figure 6 in Rajski; Note: an LFSR is a finite-state machine to automatically generate a number of test patterns).

35 U.S.C. 103(a) rejection of claim 9.

LFSR PRPG circuits in Figures 1 and 6 are connected to Combinational Phase Shifter logic between the LFSRs and the scan chains to decompress test patterns.

35 U.S.C. 103(a) rejection of claims 22-26, 28, 29, 61 and 62.

Nadeau-Dostie1, Nadeau-Dostie2 and Rajski substantially teaches the claimed invention described in claims 1-20 (as rejected above).

However Nadeau-Dostie1, Nadeau-Dostie2 and Rajski do not explicitly teach the specific use of combinational logic.

The Examiner asserts that use of specific hardware component does not deviate from the scope or the intent of the teachings in the Nadeau-Dostie1, Nadeau-Dostie2 and

Rajski patents since one of ordinary skill in the art at the time the invention was made would have known how to design the components in the Nadeau-Dostie1, Nadeau-Dostie2 and Rajski patents using common combinational logic base on design requirements for proper operation and obvious engineering design choices given the design requirements.

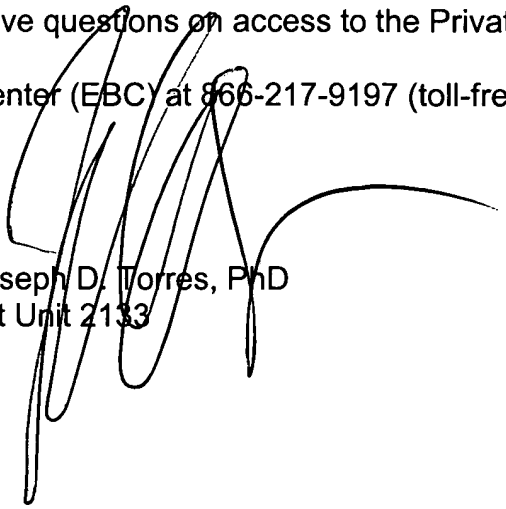
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nadeau-Dostie1, Nadeau-Dostie2 and Rajski by including use of combinational logic. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of combinational logic would have provided the opportunity to implement the design taught in the Nadeau-Dostie1, Nadeau-Dostie2 and Rajski patents using common combinational logic base on design requirements and obvious engineering design choices given the design requirements.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133